ELEC 2120-005
Lab 8 – Convolution TIMS Wk 1
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INTRODUCTION
The purpose of this lab is to get a hands-on experience with convolution to understand what is physically happening in regard to the mathematical formula given in lecture. Additionally, this lab looked at special convolution properties applying to sinewaves and analyzed a filter operating in the time domain.

PART 1
The goal of part 1 was to generate the desired INPUT signal for the system shown below in Figure 1. This INPUT signal was a 1V amplitude pulse with a width of 1ms. To generate this signal, the SYNC output from the sequence generator, which provides a 5V pulse, was connected to a triple adder with a0 gain of 0.243 to achieve a 1V amplitude pulse. To achieve the 1ms pulse width, the 8.33kHz TTL master signal was divided using the DIGITAL UTILITIES. The 8.33kHz was first divided by 4 to produce a 2kHz signal which was then divided by 2 to get the target 1kHz signal. This 1kHz was connected to the clock input of the sequence generator.

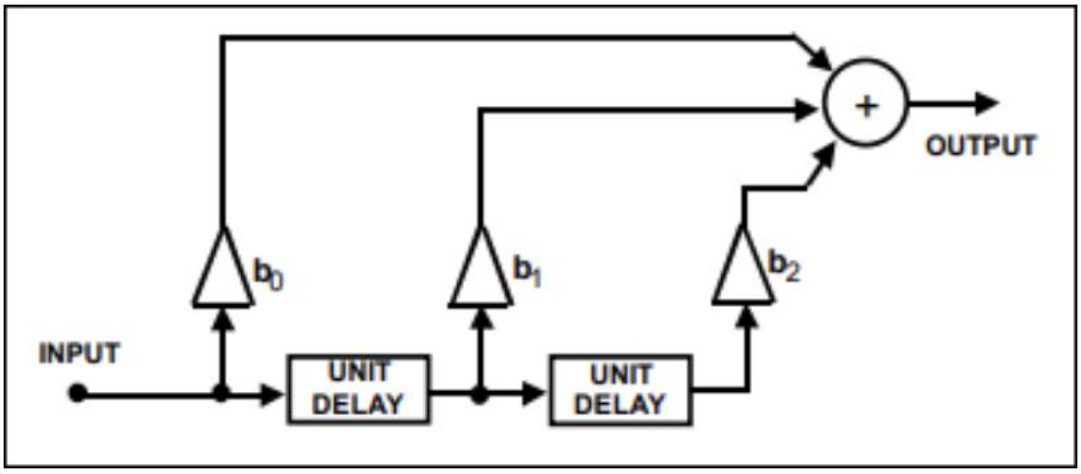

Figure 1. System block diagram

The INPUT signal measured on the scope is shown below in Figure 2. The multiple time divisions of the input clock signal results in one pulse every 32 periods.

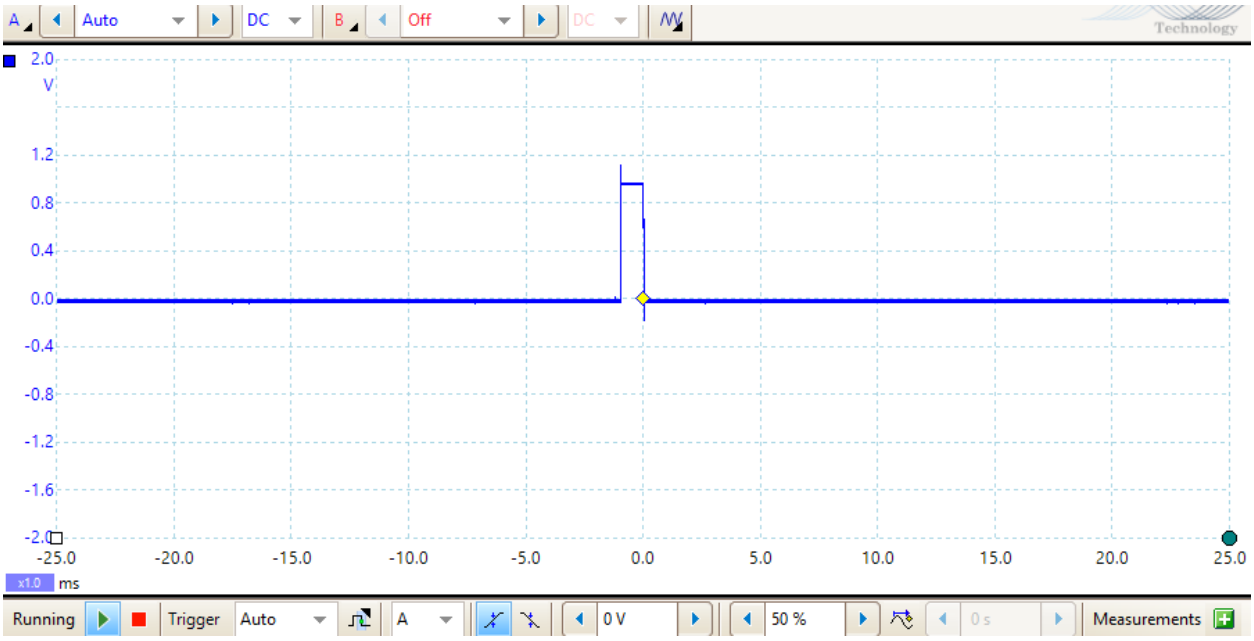

Figure 2. Scope output

PART 2

Part 2 looked at the unit pulse response of the system shown in figure one. This is the system response due to all three inputs entering the triple adder with gains b0 = 0.3, b1 = 0.5, b2 = -0.2. The scope output of the unit step response is shown below in figure three. The output appears as three different pulses of various amplitudes. These amplitudes are listed below.

- h[0] = 0.261 V
- h[1] = 0.423 V
- h[2] = -0.237V

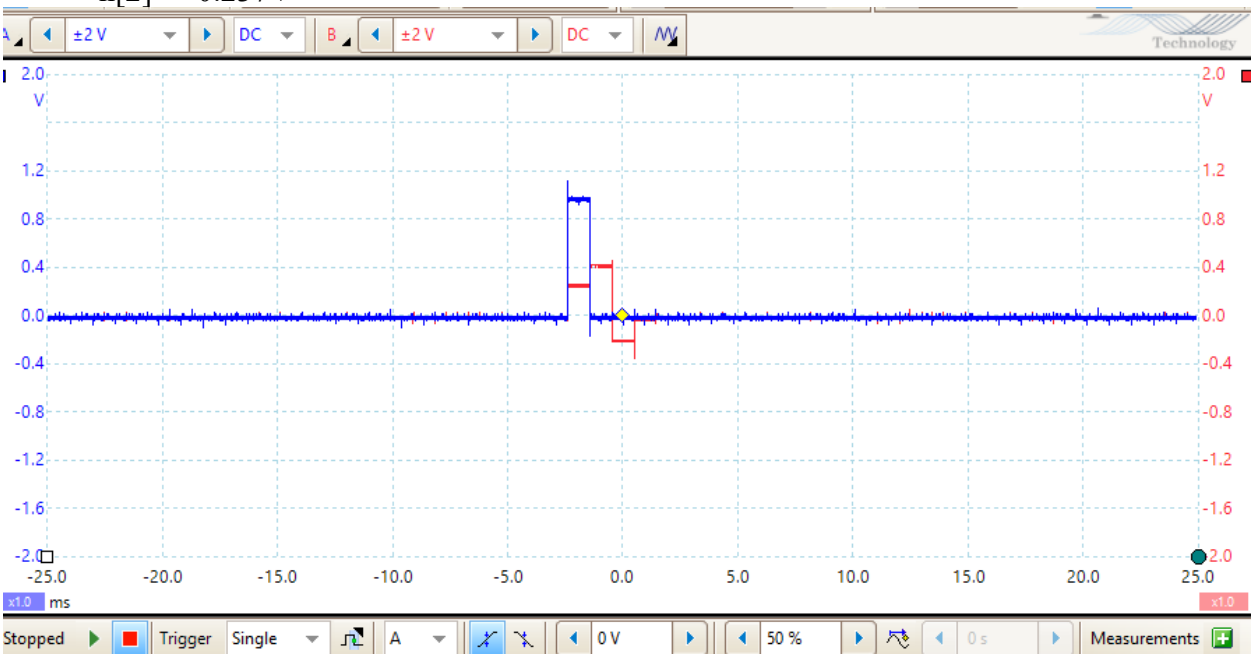

Figure 3. Scope Output of Unit Step Response

PART 3

Part 3 examined the superposition sum of the step response. The sequence generator clock rate was halved to 500 Hz. The output signal appears as four nonzero pulses per frame. The amplitudes of these pulses are shown below. Figure 4 shows the superposition of the original step response(blue) with the time shifted step response(red) to form the overall signal (purple) which matches the scope output. Note each gridline represents 0.1V.

A1 = 0.255V
A2 = 0.648 V
A3 = 0.235 V
A4 = -0.251 V

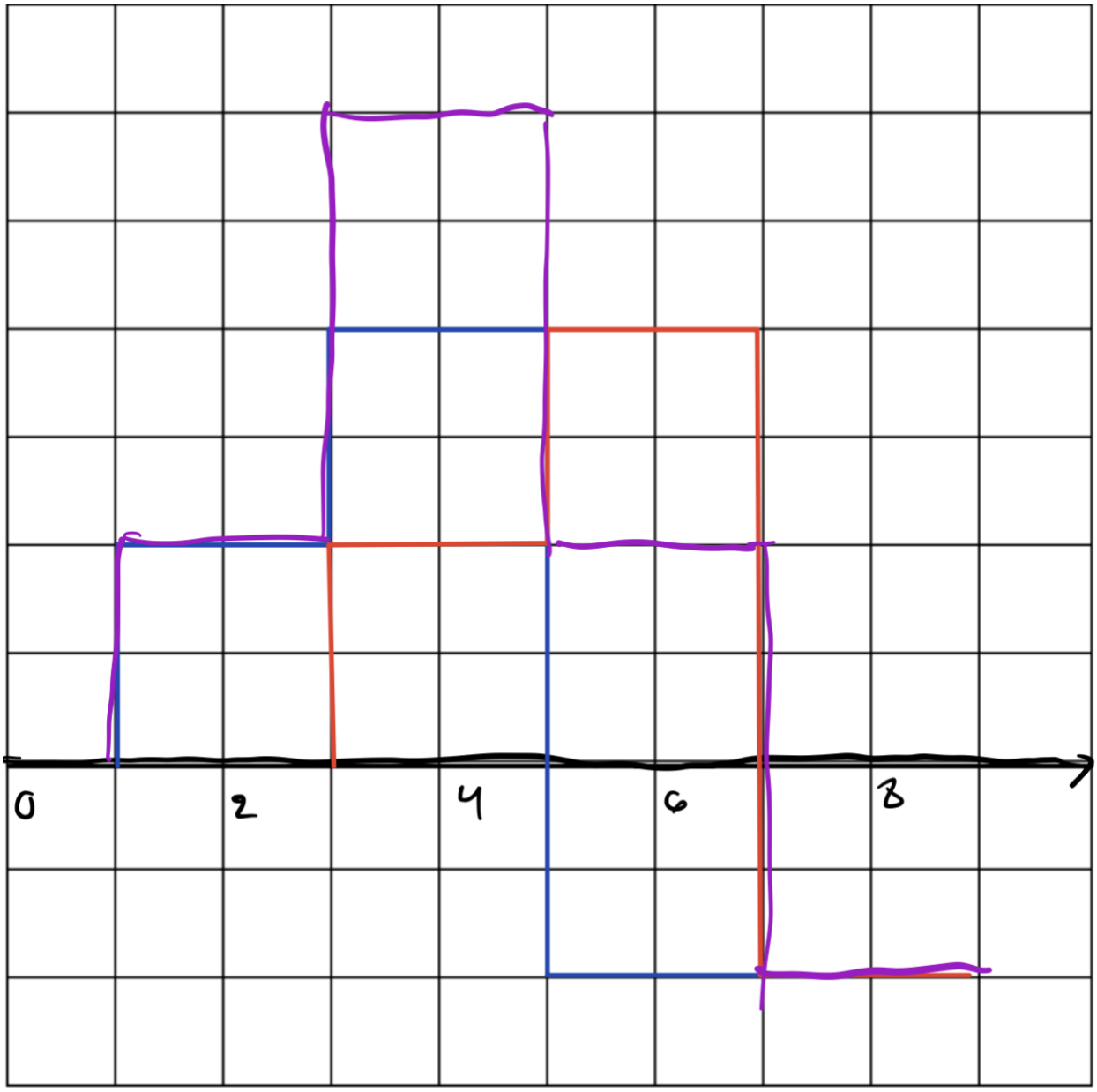

Figure 4. Superposition in Part 3

PART 4

The final exercise examines the same system but now using a rectified sine wave as the input. This signal was obtained from the ARB 1 output. The ARB 1 output was passed through a rectifier and was then passed to the sample/hold block which converted the signal to a discrete sequence of pulses. The clock signal was obtained from ARB 2. The peak-to-peak voltage was measured at 3.86Vpp and 100Hz. The rectifier is used to produce a positive output voltage for both the positive and negative half cycles of the sine input wave. This changes the amplitude. A sketch of the original half-rectified sinusoid and the discrete output from SAMPLE/HOLD is shown below in Figure 5

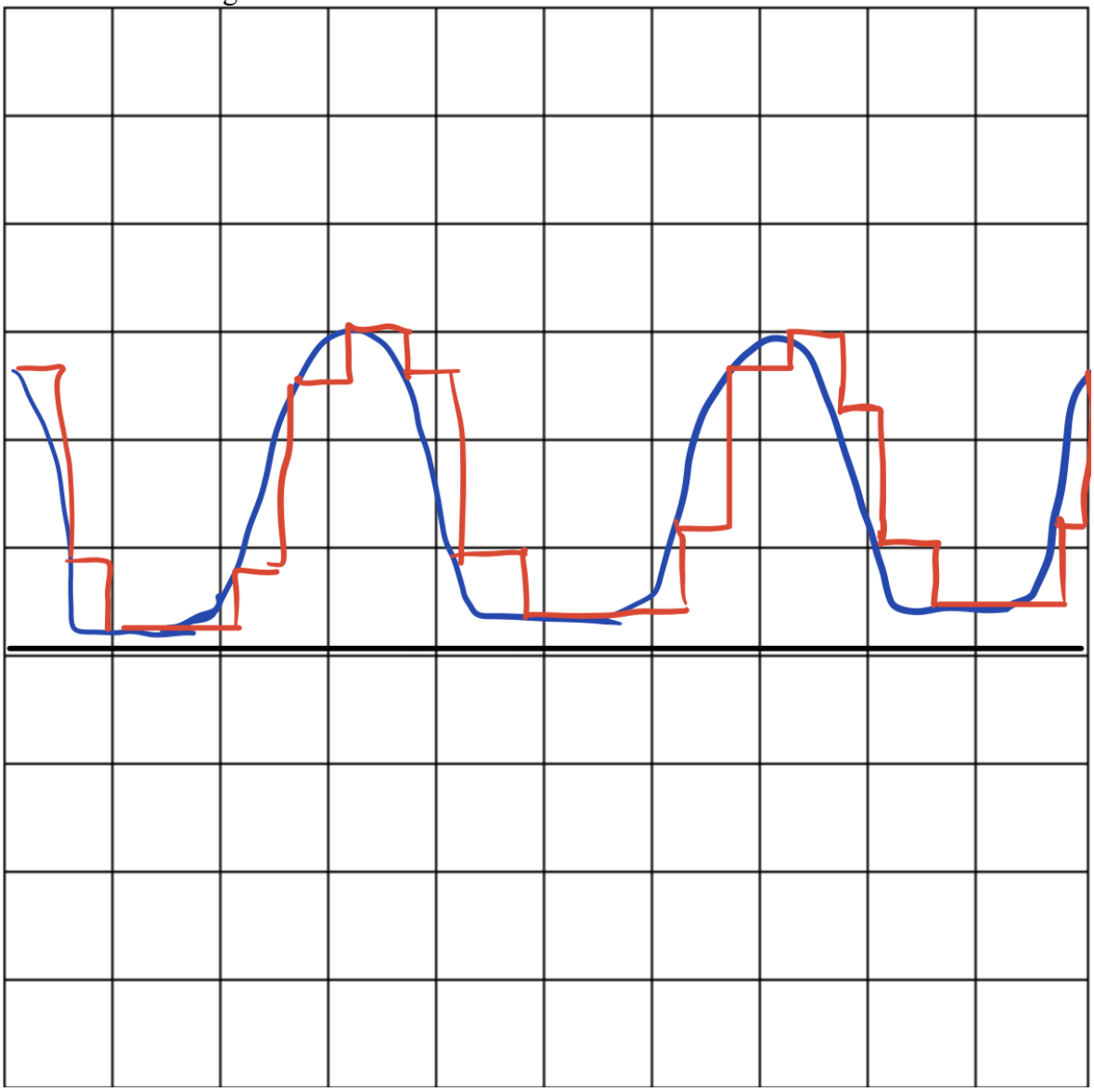

Figure 5. Half-Rectified Sinusoid and S/H output

As shown above, sample and hold seems to sample the input signal at a certain time. Then hold the sampled value as a discrete signal until it samples the input again.

CONCLUSION

In conclusion, seeing how the unit step responses superimposed to form the final system output was interesting. I had some issues with getting the triple adder module to function properly. No major improvements for this lab